APPLICATION

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TITLE: PROGRAMMABLE GAIN VOLTAGE BUFFER

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BACKGROUND

[0001] Integrated circuits often require substantially constant bias voltages. A voltage reference circuit may be used to generate a precise voltage for use by other circuits. However, when more than one load circuit shares the same voltage reference, the collective load capacitance imposed by such circuits on the voltage reference can be substantial. Furthermore, some of the load circuits may involve transistor switching and/or coupling and decoupling capacitors to and from the voltage reference, both of which may result in large current spikes being drawn from the voltage reference.

[0002] A voltage buffer may be used to buffer voltages between the reference circuit and the load circuits. A programmable gain voltage buffer, which has a programmable gain, may be use to provide a stable reference voltage over a variety of circuit conditions.

SUMMARY

[0003] The present application relates to a programmable gain voltage buffer, which may be implemented in a variety of electrical devices and systems. The programmable gain voltage buffer may be particularly suitable for a deep sub-

micron and high speed circuit with relatively low load resistance values and large current values in small circuit geometries.

[0004] An aspect of the application relates to a system comprising a voltage buffer. The voltage buffer comprises first, second, third and fourth transistors and first and second resistors. The first and second transistors are configured to receive first and second input signals, respectively. The first resistor is coupled to the first transistor. The second resistor is coupled to the second transistor. The third transistor is coupled in parallel with the first resistor. The fourth transistor is coupled in parallel with the second resistor. The third and fourth transistors are configured to receive control signals to adjust a voltage gain of (a) a first output point between the first transistor and the first resistor, and (b) a second output point between the second transistor and the second resistor.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Fig. 1 illustrates an example of a conventional programmable gain voltage buffer.

[0006] Fig. 2 illustrates another example of a programmable gain voltage buffer.

[0007] Fig. 3 illustrates a programmable gain voltage buffer according to an embodiment.

[0008] Fig. 4 illustrates a loop circuit that may be implemented with the buffer circuit in Fig. 3.

[0009] Fig. 5 illustrates a method of using the programmable gain voltage buffer of Fig. 3.

[0010] Fig. 6 illustrates a device with a programmable gain voltage buffer circuit.

DETAILED DESCRIPTION

[0011] Fig. 1 illustrates an example of a conventional programmable gain voltage buffer circuit 100. The programmable gain voltage buffer may be used to buffer voltages between two circuits, e.g., a voltage reference circuit and one or more load circuits. The programmable gain voltage buffer has a gain that may be controlled to change in programmable gain steps.

[0012] Input lines 134A and 134B may receive a differential input signal, e.g., two voltage signals equal in magnitude but out of phase. Output points 136A and 136B may each provide an output signal with a gain. If the difference between both output points 136A, 136B is taken as an output, the differential gain effectively doubles relative to the individual gain which would exist between

one input 134A and one output point 136A, because the individual gains are out of phase.

[0013] The gain of the programmable gain voltage buffer circuit 100 depends on the total equivalent resistance seen by the output points 136A and 136B. The total equivalent resistance (and the gain) may be adjusted by switching transistors (S1) 104, 106 and transistors (S2) 102, 108 ON and OFF to effectively insert or remove resistors (R1) 122, 124 and resistors (R2) 120, 126 from the circuit 100.

[0014] A disadvantage of the programmable gain voltage buffer circuit 100 of Fig. 1 is the relatively large area required by the four resistors 120-126. Also, the transistors 102-108 may need to be relatively large, increasing the parasitic capacitance, which may slow down the circuit.

[0015] Fig. 2 illustrates a variation of the programmable gain voltage buffer circuit 100 in Fig. 1. The programmable gain voltage buffer circuit 200 uses transistors (t1) 204, 206 and transistors (t2) 202, 208 as variable resistors. Switching of the transistors ON and OFF controls the resistance at output points 236A and 236B, and thus the gain of the buffer circuit 200. However, the source-drain resistances (R_{SD}) of the t1 transistors 204, 206 and t2 transistors 202, 208 are nonlinear, and thus the

control of the variable resistance (and gain) may be inaccurate.

[0016] Fig. 3 illustrates a programmable gain voltage buffer circuit 300 according to an embodiment. The gain of the programmable gain voltage buffer circuit 300 depends on the total equivalent resistance seen by the output points 334A and 334B. In this circuit, the primary resistance is provided by resistors (R1) 306 and 308. Transistors (t1) 304, 314 and transistors (t2) 302, 316 are utilized as variable resistances to adjust the effective resistance value seen at the output points 334A and 334B. For example, when the t1 and t2 resistors 304, 302 and an input transistor 310 on the left side of the circuit are turned on, the equivalent resistance at the output point 336A is equal to the resistor 306 in parallel with the inherent resistances of the transistors 302, 304, 310. The equivalent resistance may be expressed as:

$$R_{equivalent} = R_{SD\ transistor\ 302} \,||\, R_{SD\ transistor\ 304} \,||\, R_{resistor\ 306} \,||\, R_{SD\ transistor\ 310}$$

$$= ((1/R_{SD\ transistor\ 302}) + (1/R_{SD\ transistor\ 304}) + (1/R_{resistor\ 306}) + (1/R_{SD\ transistor\ 310}))^{-1}$$

[0017] Each resistor 306, 308 may have a resistance R (e.g., 1 kOhm). Each transistor 302, 304, 314, 316 may have an inherent source-drain resistance of, e.g., R, R/2,

or R/4 kOhms (e.g., 1 kOhm, 500 Ohms, or 250 Ohms), which correspond to programmable gain steps of 1, 1/2, or 1/4, respectively. By adjusting the resistance ratio of the transistors, different programmable gain steps can be achieved.

[0018] Adding more pairs of transistors in parallel with the resistors 306, 308 may provide a larger programmable gain control, but also increases the total size of the circuit 300, which may slow down the circuit. Fig. 3 only shows two pairs of transistors 302, 316 and 304, 314, but any number of pairs of transistors may be added in parallel with the resistors 306, 308.

[0019] The programmable gain voltage buffer circuit 300 of Fig. 3 may have several advantages over the buffer circuits shown in Figs. 1 and 2.

[0020] Since the resistors 306, 308 in the buffer circuit 300 predominate, the t1 transistors 304, 324 and t2 transistors 302, 316 do not substantially affect the accuracy of the equivalent resistance. This provides accurate programmability without requiring physically large resistors.

[0021] The current through the resistors 306, 308 in Fig. 3 may be smaller than the current through the resistors 120-126 in Fig. 1 because most current flows

through the t1 and t2 transistors. In deep sub-micron technology the contacts of the devices (e.g., transistors, resistors, etc.) are getting smaller and smaller, causing the current carrying capability of each contact to become smaller as well (typical around 0.2mA/contact). However, in high speed applications, large currents (e.g., multi-mA) may be necessary. For a given resistance value, a transistor normally has a larger width than a resistor does, which allows a transistor to have more contacts than a resistor. More contacts allow a transistor, such as the transistor 304, to carry more current easier than a resistor, such as resistor 306. The transistors 102-108 in Fig. 1 are in series with the resistors 120-126, and the current must go through the resistors 120-126, which limits the total current level. In contrast, the transistors 302, 304, 314, 316 in Fig. 3 are in parallel with the resistors 306, 308, and the majority of current flows through these transistors instead of the resistors 306, 308. Thus, the current through the resistors 306, 308 in Fig. 3 can be much smaller than the current through the resistors 120-126 in Fig. 1.

[0022] The buffer circuit 300 in Fig. 3 may also provide a more accurate gain control than the buffer circuits 100 and 200 in Figs. 1 and 2 because of the linear resistances

of the resistors 306, 308, which are in parallel with the t1 transistors 304, 314.

[0023] The resistors 306, 308 in Fig. 3 may be smaller in size than the resistors 122, 124 in Fig. 1 since they only need to carry a smaller current. In addition, the t1 transistors 304, 314 in Fig. 3 may be smaller in size and have more current capability than the S1 transistors 104, 106 and S2 transistors 102, 108 in Fig. 1. The buffer circuit 300 in Fig. 3 as a whole may be smaller in size than the buffer circuits 100 and 200 in Figs. 1 and 2. The smaller size may result in less parasitic capacitance, which may improve the speed of the circuit and lower power consumption.

[0024] Fig. 4 illustrates a loop circuit 400 that may be coupled to the buffer circuit 300 in Fig. 3 to adjust or control the accuracy of the gain. The loop circuit 400 includes an output line 414, a resistor 402, a tunable resistor 404, a capacitor 406, an operational amplifier (op amp) 408, a first current source 410 and a second current source 412. The first current source 410 may provide the same amount of current as the second current source 412.

[0025] The resistor 402 may be referred to as a "reference". The voltage drop across the reference resistor 402 is equal to the current source 410 multiplied

by the resistance of resistor 402, i.e., $V = I_{source410}R_{402}$. The tunable resistor 404 may be referred to as a "master", which follows the reference resistor 402. The voltage drop across the variable resistor 404 may be expressed as $V = I_{source412}R_{Tune404}$. The control loop will force $I_{source410}R_{402} = I_{source412}R_{Tune404}$ since $I_{source410} = I_{source412}$. Thus, $R_{402} = R_{tune404}$, i.e., the control loop will force the master tunable resistor 404 to track the reference resistor 402.

[0026] The output line 414 of the operational amplifier 408 may be coupled to the capacitor 406 and may control the resistance of the tunable resistor 404 so that $R_{402} = R_{Tune404}$ remains valid across process and temperature variations. The output line 414 may be coupled to the control gates 322A, 322B, 332C, and 322D of the transistors 302, 304, 314, and 316 in Fig. 3 to provide a bias voltage. These transistors may be referred to as "slave" resistors because they share the same gate bias voltage as the master resistor 404 and therefore their resistances match the resistance of the master resistor 404, which tracks the reference resistor 402.

[0027] Fig. 5 illustrates a method of using the programmable gain voltage buffer circuit 300 of Fig. 3. An input signal is applied to a voltage buffer 300 at 500. Pair(s) of transistors (302,316 and/or 302,314) parallel to

the pair of resistors 306, 308 in the voltage buffer 300 are activated to control the gain of the voltage buffer 300 at 502. The voltage buffer 300 provides an output signal with the programmed gain at 504.

[0028] Fig. 6 illustrates a device 600 with a programmable gain voltage buffer circuit 300 of Fig. 3. The buffer circuit may be coupled between two or more circuits, e.g., a voltage reference circuit 605 and a number of load circuits 610. The buffer circuit 300 may receive an input signal from the voltage reference circuit 605 and output a signal substantially equal to the input signal multiplied by a programmable gain. A control circuit 615 may control the programmable gain of the buffer circuit 300.

[0029] The programmable gain voltage buffer may be implemented in a variety of electrical devices and systems. The programmable gain voltage buffer may be particularly suitable for a circuit with relatively low resistance values and large current values in small circuit geometries.

[0030] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the application. For example, steps in the

flowchart may be skipped or performed out of order.

Accordingly, other embodiments are within the scope of the following claims.